REMARKS

Applicants respond hereby to the outstanding Office action dated August 3, 2007. A Petition For Extension of Time accompanies this Amendment to extend the time for applicants' response, up to and including December 3, 2007. Applicants have amended claims 1, 12 and 13. Claims 1-20 are pending hereinafter, where claims 1 and 13 are the independent claims.

At paragraphs 1 and 2 of the outstanding Office Action, Fig. 1 was objected to (MPEP §608.02) for lack of a legend "Prior Art," and all of the drawings were objected to under 37 CFR 1.83(a), the Examiner asserting that the limitations of claims 3 and 9 are not found. At paragraphs 3 and 4 of the outstanding Office action, claims 1-20 were rejected under 35 USC §112, Second Paragraph, as indefinite. At paragraphs 5 and 6 of the outstanding Office action, the Examiner rejected claims 1-5 and 11-17 under 35 USC §102(b) as anticipated by US Patent No. 5,880,983 to Elliot, et al. (Elliot). At paragraphs 9 and 10 of the outstanding Office Action, the Examiner rejected claims 6-8 and 18-19 under 35 USC §103(a) as unpatentable over Elliot in view of US Patent No. 7,228,325, to Wilson, et al. (Wilson).

Drawing Objections

In response to the objection to Fig. 1, applicants have amended Fig. 1 to clearly indicate "Prior Art," as shown in the "replacement sheet" accompanying this Amendment. In response to the objections under 37 CFR 1.83(a), applicants respectfully assert that the limitations of claims 3 and 9. Applicants respectfully assert that the aligner and multiplexer of claim 3 are shown in Fig. 2 and 3, and the test result number, including a first of the bits and a second of the bits are shown in Figs. 4-8. Applicants respectfully assert that the drawings comply with 37 CFR 1.83(a),

and request withdrawal of the drawing objections.

Rejections Under 35 USC §112

In response to the rejection of claims 1-20 under 35 USC §112, second paragraph, applicants' have amended claims 1, 12 and 13. For example, claims 1 and 13 now recite the aligner as aligning (the aligner aligns), and claim 12 is amended to identify, and provide antecedent support for the "ea + eb – 2eb" (: [exponent ea + exponent eb – exponent 2eb]). Accordingly, applicants respectfully assert that claims 1-20 now fully comply with 35 USC §112, second paragraph, and request withdrawal of the rejection of claims 1-20 thereunder.

Rejections Under 35 USC §101

In response to the rejection of claims 1-20 under 35 USC §101, as directed to non-statutory subject matter, applicants respectfully assert that claims 1-20 comply fully with Section 101. At paragraph 6 of the outstanding Office action, the Examiner asserts that claims 1-20 recite a method and unit for performing multiplying/adding operation without further disclosing a practical/physical application, or useful and tangible result since the claims "preempt" every substantial practical application of the "idea" embodied by the claim, and that there is no cited limitation that breathes sufficient life and meaning into the preamble to limit to a particular application. Applicants respectfully disagree.

Applicants' claims 1 and 13 set forth a floating point execution unit for performing multiply/add operations using a plurality of operands taken from an instruction having a plurality of operand positions, and a method of operating a floating point execution unit to perform multiply/add

operations the floating point unit having a multiplier, an aligner coupled to the multiplier, and a multiplexer. The subject matter of independent claims 1 and 13, and claims 2-12, and 14-20, which depended therefrom, are directed to a machine and process, respectively. The subject matter of claims 1-20 do not stand outside the scope of Section 101 because same claims do not comprise an abstract idea, law of nature or natural phenomenon. Applicants claim a floating point execution unit and a method of operating a floating point execution unit.

Applicants' floating point execution unit (claim 1) and method of operating a floating point execution unit (claim 13), increase the performance speed of a floating point execution unit (applicants' Specification at page 2, paragraph [0007]). Applicants' invention as claimed removes operand formatting/selection and unpacking from the timing critical path in floating point execution, increasing performance of the floating point unit significantly (applicants' Specification at page 2, paragraph [0008]). Applicants' claims 1-20 do not attempt to patent a principle, but a novel floating point unit, and a novel method of operating a floating point unit. Applicants are not attempting to patent the concept of floating point arithmetic, or "every" floating point execution unit, but only a floating point execution unit, and method of operating a floating point execution unit, as set forth in claims 1-12, and 13-20, respectively, including all of the features and limitations of those claims.

The inventions perform multiply/add operations using a plurality of operands taken from an instruction having a plurality of operand positions. As such, the claims provide a useful, tangible, concrete result under the law. MPEP 2106. A floating point execution unit, and method, that operates on a plurality of operands, for example, "multiplying to calculate a product of two of the operands" is a utility that is specific, substantial and credible under the law. MPEP 2106(a). The inventive operation of performing multiply/add operations using a plurality of operands provides the

floating point output in less time than known floating point execution units, and known methods of operating a floating point execution unit. The floating point execution unit output is a concrete, tangible result (MPEP 2106(a). MPEP 2106(b)).

Accordingly, applicants respectfully assert that claims 1-20 are statutory under 35 USC §101, and request withdrawal of the rejection of claims 1-20 thereunder.

Rejections Under 35 USC 102(b)

Claims 1-5 and 11-17 were rejected under 35 USC §102(b) as anticipated by Elliot. The Examiner asserts that Elliot at Fig. 2 discloses a floating point execution unit (Fig. 2) for performing multiply multiply/add operations using a plurality of operands taken from an instruction with a plurality of operand positions (A, B and C; col. 1, lines 21-50), the floating point execution unit comprising:

a multiplier 102 for calculating a product of two operands (Elliott's operands A and C);

an aligner 118 coupled to the multiplier 102 for combining the product and a third (B) of the operands;

a first data path for supplying to the multiplier operands from a first and second of the operand positions of the instruction (Data feed path feeding A and C into multiplier 102);

a second data path for supplying to the third operand to the aligner (data path feeding B into muxes 114, 116; and

a multiplexer (114, 116) on the second data path for selecting, for use by the aligner, either the operand from the second operand position of the instruction (A) or the operand from the third operand position of the instruction (B).

Applicants respectfully disagree. Applicants independent claims 1 sets forth a floating point execution unit for performing multiply/add operations using a plurality of operands taken from an instruction having a plurality of operand positions, the floating point unit comprising:

a multiplier for calculating a product of two of the operands;

an aligner coupled to the multiplier for aligning said product and a third of the operands;

a first data path for supplying to the multiplier operands from a first and a second of the operand positions of the instruction;

a second data path for supplying the third operand to the aligner; and

a multiplexer on the second data path for selecting, for use by the aligner, either the operand from the second operand position of the instruction or the operand from the third operand position of the instruction.

Elliott discloses a floating point split multiply/add system with infinite precision. The Examiner asserts that Elliot discloses a second data path for supplying the third operand to the aligner (data path for feeding B into muxes 114 and 116 of Fig. 2A). The Elliot data path that feeds B into muxes 114 and 116 is not equivalent to applicants' second data path. For example, applicants Fig. 3 shows a data path to the aligner that includes no muxes. For that matter, while the Examiner asserts that Elliott discloses a multiplexer on the second data path for selecting, for use by the aligner, either the operand from the second operand position of the instruction or the operand from the third operand position of the instruction, applicants disagree. Elliot does not disclose a

multiplexer on the second data path for selecting, for use by the aligner, either the operand from the second operand position of the instruction or the operand from the third operand position of the instruction. Elliot muxes only A & B, and the multiply output AC.

Applicants, therefore, respectfully assert that Elliot does not include each of the elements of applicants' independent claims 1 and 13, and independent claims 1 and 13 are patentable under Section 102(b) in view of Elliott. Claims 2-12 depend from claim 1 and are patentable therewith, and claims 14-20 depend from claim 13 and are patentable therewith. Hence, applicants respectfully request withdrawal of the rejection of claims 1-20 under section 102(b) in view of Elliott.

Rejections Under 35 USC §103(a)

Claims 6-8 and 18-19 were rejected under 36 USC §103(a) as unpatentable over Elliott in view of Willson. The Examiner asserts that Elliott fails to disclose that each of the operands has an exponent value, and further comprises means, operating in parallel with the multiplier and the aligner, to determine whether the exponent values of any of the operands is 0 while the multiplier calculates the product to establish a test result number," but that Willson does, and that it would have been obvious in order to conserve power to combine Willson's feature at col. 7, line 60-col. 8, line 15, with Elliott to realize the invention as set forth in claims 6-8 and 18-19. Applicants respectfully disagree.

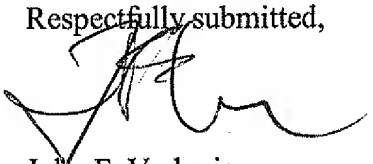
As mentioned above in response to the rejection of independent claims 1 and 13 under Section 102(b) in view of Elliott, Elliot does not teach each of the limitations, or the equivalents, of applicants' claims 1 and 13. Because Elliott does not anticipate claims 1 and 13 under the law, Elliot

does not include each of the limitations of claims 1 and 13. Hence, combining Elliott with Willson, even assuming arguendo that Willson includes the limitations as asserted in paragraph 10, cannot realize applicants' invention as set forth in claims 6-8 and 18-19 for at least the reasons set forth above for the patentability of claims 1 and 13 in view of Elliott under Section 102(b). Applicants respectfully request, therefore, that the rejection of claims 6-8 and 18-19 under section 103(a) over Elliott in view of Willson be withdrawn.

Conclusion

It follows that each of pending claims 1-20 are patentably distinct from Elliott, whether under Section 102(b) or combined with Willson under Section 103(c). If the Examiner believes that a telephone conference with applicant's attorneys would be advantageous to the disposition of this case, the Examiner is asked to telephone the undersigned.

Respectfully submitted,



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